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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WATKO, JULIE ANNE	

ART UNIT	PAPER NUMBER
2627	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,844	SUTARDJA, PANTAS	
	Examiner	Art Unit	
	Julie Anne Watko	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) *61-66* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/08/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group I, claims 1-60, in the reply filed on September 19, 2006, is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

2. The disclosure is objected to because of the following informalities:

On page 5, ¶ 0013, the specification recites "current sources 50 and 52". This is inconsistent with ¶ 0011, which recites "current sources 42 and 44".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 36, 42 and 55-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 36 recites the limitation "said transistor" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim 42 recites the limitation "said first voltage limiting means" in lines 1-2. There is insufficient antecedent basis for this limitation in the claims.

Claim 55 recites the limitation "said shunting device" in line 2. There is insufficient antecedent basis for this limitation in the claims.

Claim 56 recites the limitation "said shunting device" in line 2. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 6, 11-12, 14, 19, 24-25, 27, 32, 37-38, 40, 45, 50-51, 53 and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Schuelke et al (US Pat. No. 6005733).

Similar dependent claims are treated together.

As recited in independent claim 1, Schuelke et al show a magnetic storage system ("disc drive", see col. 1, line 8), comprising: a read element R_{MR}; and an electrostatic discharge (ESD) protection circuit (see Fig. 1) that comprises a shunting device (including S1 and S2) including a first terminal 12 that communicates with a first terminal of said read element and a second terminal 14 that communicates with a second terminal of said read element, wherein said shunting device is conductive when said read element is disabled (see col. 4, lines 52-53, "shorting switches S1 and S2 are closed when R_{MR} is not selected to perform a read operation") and nonconductive when said read element is enabled (see col. 5, lines 1-4, "control circuit 22

only opens the pair of shorting switches S1 and S2 when R_{MR} is selected to perform a read operation").

As recited in independent claim 14, Schuelke et al show an electrostatic discharge (ESD) protection circuit for a read element R_{MR} (see Fig. 1) in a magnetic storage system ("disc drive", see col. 1, line 8), comprising: a shunting device that includes: a first terminal 12 that communicates with a first terminal of the read element R_{MR}; and a second terminal 14 that communicates with a second terminal of the read element R_{MR}, wherein said shunting device provides a conductive path between said first and second terminals of said shunting device when the read element is disabled (see col. 4, lines 52-53, "shorting switches S1 and S2 are closed when R_{MR} is not selected to perform a read operation") and a nonconductive path between said first and second terminals of said shunting device when the read element is enabled (see col. 5, lines 1-4, "control circuit 22 only opens the pair of shorting switches S1 and S2 when R_{MR} is selected to perform a read operation").

As recited in independent claim 27, Schuelke et al show a magnetic storage system ("disc drive", see col. 1, line 8), comprising: reading means R_{MR} for reading magnetic fields; and electrostatic discharge (ESD) protecting means (see Fig. 1) that comprises a shunting means (including S1 and S2) for shunting and including a first terminal 12 that communicates with a first terminal of said reading means and a second terminal 14 that communicates with a second terminal of said reading means, wherein said shunting means is conductive when said reading means is disabled (see col. 4, lines 52-53, "shorting switches S1 and S2 are closed when R_{MR} is not selected to perform a read operation") and nonconductive when said reading means is

enabled (see col. 5, lines 1-4, "control circuit 22 only opens the pair of shorting switches S1 and S2 when R_{MR} is selected to perform a read operation").

As recited in independent claim 40, Schuelke et al show an electrostatic discharge (ESD) protecting circuit (see Fig. 1) for a read element R_{MR} in a magnetic storage system ("disc drive", see col. 1, line 8), comprising: shunting means (including S1 and S2) for protecting the read element from ESD and that includes: a first terminal 12 that communicates with a first terminal of the read element; and a second terminal 14 that communicates with a second terminal of the read element, wherein said shunting means provides a conductive path between said first and second terminals of said shunting means when the read element is disabled (see col. 4, lines 52-53, "shorting switches S1 and S2 are closed when R_{MR} is not selected to perform a read operation") and a nonconductive path between said. first and second terminals of said shunting means when the read element is enabled (see col. 5, lines 1-4, "control circuit 22 only opens the pair of shorting switches S1 and S2 when R_{MR} is selected to perform a read operation").

As recited in independent claim 53, Schuelke et al show a method of operating a magnetic storage system ("disc drive", see col. 1, line 8), comprising: reading magnetic fields (see col. 5, lines 1-4, "perform a read operation") using a read element R_{MR} having first and second terminals (see terminals connected to 12 and 14 in Fig. 1); and shorting said first and second terminals of said read element when said reading means is disabled (see col. 4, lines 52-53, "shorting switches S1 and S2 are closed when R_{MR} is not selected to perform a read operation").

As recited in claims 6, 19, 32 and 45, Schuelke et al show first and second current sources (24 and 26), wherein said first terminal (near 12) of the read element and said first

terminal 12 of said shunting device communicate with said first current source 24 and wherein said second terminal (near 14) of said read element and said second terminal 14 of said shunting device communicate with said second current source 26.

As recited in claims 11 and 37, Schuelke et al show a preamp means 10 for amplifying a signal output by said reading means, wherein said ESD protecting means is implemented in (see Fig. 1) said preamp means 10 of said magnetic storage system.

As recited in claims 12, 25, 38, 51 and 59, Schuelke et al show that said read element is one of a magneto-resistive (MR) sensor R_{MR}, a giant magneto-resistive (GMR) sensor, and a tunneling giant magneto-resistive (TGMR) sensor.

As recited in claims 24 and 50, Schuelke et al show a magnetic storage system (see Fig. 1) comprising the ESD protection circuit (including S1 and S2) and further comprising said read element RMR.

7. Claims 1, 9-10, 12, 14, 22-25, 27, 35-36, 38, 40, 48-51, 53 and 57-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Voldman (US PAP No. 20020097532 A1).

As recited in independent claim 1, Voldman shows a magnetic storage system (see Fig. 1), comprising: a read element 12; and an electrostatic discharge (ESD) protection circuit 11 that comprises a shunting device 32 including a first terminal MR(+) that communicates with a first terminal of said read element 12 and a second terminal MR(-) that communicates with a second terminal of said read element 12, wherein said shunting device is conductive when said read element is disabled ("During an ESD event the gate voltage is pulled relatively high if the gate is being used as a trigger for turn-on. The substrate/body voltage source 36 is relatively high during an ESD event which lowers the turn-on voltage through the reverse body effect. ... Increasing

the substrate/body voltage increases conduction by lowering the turn-on threshold of the MOSFET 32 through the reverse body effect", see ¶ 0020; see also ¶ 0026, "Above this turn-on voltage for the array, the resistance becomes low which adds to the over-voltage protection") and nonconductive when said read element is enabled ("presents a high resistance to the leads 14A, 14B for up to two times the junction voltage for the diodes", see ¶ 0026).

As recited in independent claim 14, Voldman shows an electrostatic discharge (ESD) protection circuit 11 for a read element 12 in a magnetic storage system (see Fig. 1), comprising: a shunting device (see Fig. 1) that includes: a first terminal MR(+) that communicates with a first terminal of the read element 12; and a second terminal MR(-) that communicates with a second terminal of the read element, wherein said shunting device provides a conductive path between said first and second terminals of said shunting device when the read element is disabled ("During an ESD event the gate voltage is pulled relatively high if the gate is being used as a trigger for turn-on. The substrate/body voltage source 36 is relatively high during an ESD event which lowers the turn-on voltage through the reverse body effect. ... Increasing the substrate/body voltage increases conduction by lowering the turn-on threshold of the MOSFET 32 through the reverse body effect", see ¶ 0020; see also ¶ 0026, "Above this turn-on voltage for the array, the resistance becomes low which adds to the over-voltage protection") and a nonconductive path between said first and second terminals of said shunting device when the read element is enabled ("presents a high resistance to the leads 14A, 14B for up to two times the junction voltage for the diodes", see ¶ 0026).

As recited in independent claim 27, Voldman shows a magnetic storage system (see Fig. 1), comprising: reading means 12 for reading magnetic fields; and electrostatic discharge (ESD)

protecting means 11 that comprises a shunting means 32 for shunting and including a first terminal MR(+) that communicates with a first terminal of said reading means and a second terminal MR(-) that communicates with a second terminal of said reading means, wherein said shunting means is conductive when said reading means is disabled ("During an ESD event the gate voltage is pulled relatively high if the gate is being used as a trigger for turn-on. The substrate/body voltage source 36 is relatively high during an ESD event which lowers the turn-on voltage through the reverse body effect. ... Increasing the substrate/body voltage increases conduction by lowering the turn-on threshold of the MOSFET 32 through the reverse body effect", see ¶ 0020; see also ¶ 0026, "Above this turn-on voltage for the array, the resistance becomes low which adds to the over-voltage protection") and nonconductive when said reading means is enabled ("presents a high resistance to the leads 14A, 14B for up to two times the junction voltage for the diodes", see ¶ 0026).

As recited in independent claim 40, Voldman shows an electrostatic discharge (ESD) protecting circuit for a read element 12 in a magnetic storage system (see Fig. 1), comprising: shunting means (including 32) for protecting the read element 12 from ESD and that includes: a first terminal MR(+) that communicates with a first terminal of the read element 12; and a second terminal MR(-) that communicates with a second terminal of the read element, wherein said shunting means provides a conductive path between said first and second terminals of said shunting means when the read element is disabled ("During an ESD event the gate voltage is pulled relatively high if the gate is being used as a trigger for turn-on. The substrate/body voltage source 36 is relatively high during an ESD event which lowers the turn-on voltage through the reverse body effect. ... Increasing the substrate/body voltage increases conduction by lowering

the turn-on threshold of the MOSFET 32 through the reverse body effect", see ¶ 0020; see also ¶ 0026, "Above this turn-on voltage for the array, the resistance becomes low which adds to the over-voltage protection") and a nonconductive path between said first and second terminals of said shunting means when the read element is enabled ("presents a high resistance to the leads 14A, 14B for up to two times the junction voltage for the diodes", see ¶ 0026).

As recited in independent claim 53, Voldman shows a method of operating a magnetic storage system, comprising: reading magnetic fields using a read element 12 having first and second terminals (see MR(+) and MR(-)); and shorting said first and second terminals of said read element when said reading means is disabled ("During an ESD event the gate voltage is pulled relatively high if the gate is being used as a trigger for turn-on. The substrate/body voltage source 36 is relatively high during an ESD event which lowers the turn-on voltage through the reverse body effect. ... Increasing the substrate/body voltage increases conduction by lowering the turn-on threshold of the MOSFET 32 through the reverse body effect", see ¶ 0020; see also ¶ 0026, "Above this turn-on voltage for the array, the resistance becomes low which adds to the over-voltage protection").

As recited in claims 9, 22, 35, 48 and 57, Voldman shows that said shunting device 11 includes a normally-on transistor 32.

As recited in claims 10, 23, 36, 49 and 58, Voldman shows that said transistor includes one of a depletion mode metal-oxide semiconductor field-effect transistor (MOSFET) 32 and a JFET.

As recited in claims 12, 25, 38, 51 and 59, Voldman shows that said read element 12 is one of a magneto-resistive (MR) sensor ("magnetoresistive sensors", see ¶ 0002), a giant magneto-resistive (GMR) sensor, and a tunneling giant magneto-resistive (TGMR) sensor.

As recited in claims 24 and 50, Voldman shows a magnetic storage system comprising the ESD protection circuit 11 and further comprising said read element 12.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-3, 15, 17, 28-29, 41, 43 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuelke et al (US Pat. No. 6005733) in view of Wang et al (US Pat. No. 6104048).

Schuelke et al show a system as recited above.

As recited in claims 2-3, 15, 17, 28-29, 41, 43 and 54, Schuelke et al are silent regarding 1st and/or 2nd voltage limiting circuits limiting voltage that is input to said 1st and/or 2nd terminals.

As recited in claims 2-3, 15, 17, 28-29, 41, 43 and 54, Wang et al show 1st and/or 2nd voltage limiting circuits (11a and 11b) limiting voltage that is input to said 1st and/or 2nd terminals (80a and 80b).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add 1st and/or 2nd voltage limiting circuits of Wang et al to the 1st and/or 2nd

terminals of Schuelke et al as taught by Wang et al. The rationale is as follows: one of ordinary skill in the art would have been motivated to add the 1st and 2nd voltage limiting circuits in order to dissipate electrostatic discharge events through the network to diminish damage to the read element so as to avoid errors in reading as taught by Wang et al (see col. 2, lines 30-35; see also col. 3, lines 18-29).

10. Claims 13, 26, 39, 52 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuelke et al (US Pat. No. 6005733).

Schuelke et al show a system as recited above.

As recited in claims 13, 26, 39, 52 and 60, Schuelke et al are silent regarding whether a voltage tolerance of said read element is less than 0.4 volts.

The law is replete with cases in which when the mere difference between the claimed invention and the prior art is some range, variable or other dimensional limitation within the claims, patentability cannot be found.

It furthermore has been held in such a situation, the Applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

It is known in the magnetic head art to routinely modify a magnetic head structure in the course of routine optimization/ experimentation and thereby obtain various standard optimized relationships including those set forth in claims 13, 26, 39, 52 and 60.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have had the magnetic head of Schuelke et al satisfy the relationships set

forth in claims 13, 26, 39, 52 and 60. The rationale is as follows: one of ordinary skill in the art would have been motivated to have had the magnetic head of Schuelke et al satisfy the relationships set forth in claims 13, 26, 39, 52 and 60 since it is known in the magnetic head art to routinely modify a magnetic head structure in the course of routine optimization /experimentation and thereby obtain various standard optimized relationships including those set forth in claims 13, 26, 39, 52 and 60. Moreover, absent a showing of criticality (i.e., unobvious or unexpected results), the relationships set forth in claims 13, 26, 39, 52 and 60 are considered to be within the level of ordinary skill in the art.

11. Claims 2-5, 7-8, 15-18, 20-21, 28-31, 33-34, 41-44, 46-47 and 55-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuelke et al (US Pat. No. 6005733) in view of Granstrom et al (US PAP No. 20030169540 A1).

Schuelke et al show a system as described above.

As recited in claims 2-3, 7, 15, 17, 20, 28-29, 33, 41, 43, 46 and 55-56, Schuelke et al are silent regarding 1st, 2nd and/or 3rd voltage limiting circuits limiting voltage input to the terminals.

As recited in claims 2-3, 7, 15, 17, 20, 28-29, 33, 41, 43, 46 and 55-56, Granstrom et al show 1st (see Fig. 10), 2nd (see Fig. 10), and 3rd (see Fig. 8) voltage limiting circuits limiting voltage input to the terminals and limiting voltage drop over the terminals.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the 1st, 2nd and 3rd voltage limiting circuits to the terminals of Schuelke et al as taught by Granstrom et al. The rationale is as follows: one of ordinary skill in the art would have been motivated to limit voltage input to the terminals and limiting voltage drop so as to

divert excess current so as to prevent breakdown of the TGMR as taught by Granstrom et al (see ¶ 0040).

As recited in claims 4-5, 8, 16, 18, 21, 30-31, 34, 42, 44 and 47, Schuelke et al are silent regarding the claimed 1st through 6th diodes and their connections to the terminals.

As recited in claims 4-5, 8, 16, 18, 21, 30-31, 34, 42, 44 and 47, Granstrom et al show 1st through 6th diodes (102, 104, 108, 106, 94 and 92, respectively).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include 1st through 6th diodes of Granstrom et al in the circuit of Schuelke et al as taught by Granstrom et al. The rationale is as follows: one of ordinary skill in the art would have been motivated to include the diodes so as to prevent magnetically and thermally induced breakdown of the TGMR as taught by Granstrom et al (see ¶ 0042).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Doss et al (US Pat. No. 6538857 B1) show a read head 130 having terminals 104 and 106 wherein said read head is protected from ESD by shorting when the read head is not being tested, and is unshorted during tests (see especially S and US in figures).

Klaassen (US Pat. No. 6400534 B1) shows a resistive shunt for ESD protection of a GMR (see col. 1, line 57-col. 2, line 39; see also col. 3, lines 15-20; see also col. 3, lines 50-62), wherein current is not shunted away from the GMR when a read test is enabled, and a low resistance bypass is enabled when testing is disabled (see col. 7, line 41-col. 8, line 18).

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julie Anne Watko whose telephone number is (571) 272-7597. The examiner can normally be reached on Monday through Friday, 1PM to 10PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dwayne D. Bost can be reached on (571) 272-7023. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Julie Anne Watko, J.D.
Primary Examiner
Art Unit 2627

October 30, 2006
JAW